

TITLE

DETECTION CIRCUIT

BACKGROUND OF THE INVENTION

Field of the Invention

5 The present invention relates to a detection circuit, and more particularly, to a plug detection circuit detecting the type of earphone connected.

Description of the Related Art

10 Normally, earphones used with personal stereos are restricted to output only, but those used with cell phones can integrate microphone function. In both cases, the earphones can implement a three-wire structure. For use with a combination cell phone/PDA, however, three-wire structure is insufficient. Thus, combination cell phone/PDA units normally employ four-wire plugs. 15 However, four-wire plugs have poor compatibility with other devices and higher cost.

20 Therefore, there is a need for an earphone jack that can detect the type of earphone connected that enables use thereof, irrespective of type.

SUMMARY OF THE INVENTION

An object of the present invention is to provide an earphone jack that can detect the type of earphone connected.

25 According to the above mentioned object, the present invention provides a plug detection circuit for detecting the type of earphone connected. The earphone plug has

plural conductive rings. In the present invention, plug detection circuit has at least one first pin and one second pin. The first pin detects whether an earphone is connected to the earphone jack, and outputs a first logic potential. The second pin detects the potential at the conductive ring of the earphone plug, and outputs a second logic potential. Plug detection circuit determines the type of earphone connected according to the first logic potential and the second logic potential.

10 **BRIEF DESCRIPTION OF THE DRAWINGS**

The present invention can be more fully understood by reading the subsequent detailed description and examples with references made to the accompanying drawings, wherein:

15 Fig. 1 is an equivalent diagram of a plug detection circuit with no earphone plug connected;

Fig. 2 is an equivalent diagram of plug detection circuit with a typical earphone plug connected;

20 Fig. 3 is an equivalent diagram of plug detection circuit with an earphone plug with microphone function connected; and

Fig. 4 shows the relationship between the detection result, the first logic potential and the second logic potential.

25 **DETAILED DESCRIPTION OF THE INVENTION**

Fig. 1 is an equivalent diagram of plug detection circuit according to the invention with no plug connected. As shown in Fig. 1, plug detection circuit of

the present invention includes resistors R1, R2, R3, R4, R5, R6, capacitors C1 and C2, and a switch S1. The earphone jack has six pins 1-6, wherein the grounding ring 10 is electrically coupled to pin 4. The resistor R1 is coupled between the voltage source Vcc and pin 1. The resistor R2 is coupled between pin 1 and the node GPIO1. The resistor R3 is coupled between pin 3 and ground. In this case, the potential at the node GPIO1 is defined as the first logic potential. Resistor R4 is coupled between the voltage source Vcc and pin 2. Resistor R5 is coupled between pin 2 and the node P1. Capacitor C2 is coupled between the node P1 and ground. Resistor R6 is coupled between the voltage source Vcc and the node GPIO2. The potential at the node GPIO2 of the resistor R6 and switch S1 is defined as the second logic potential. Switch S1 is coupled to the resistors R5 and R6 and ground. In this case, switch S1 is a MOS transistor having a gate coupled to the resistor R5 at node P1. Pin 5 and pin 6 are coupled together and pin 3 and pin 1 are coupled together when no plug is connected to the jack. At this time, the potential at node GPIO1 is a divided-voltage produced by the resistors R1 and R3. A low pass filter consists of the resistor R2 and the capacitor C1. The potential at node GPIO1 is regarded as low when the resistance of the resistor R1 exceeds that of the resistor R3. The voltage source Vcc charges the capacitor C2 through the resistors R4 and R5. Finally, the potential at node P1 is increased to voltage source Vcc to turn on switch S1, with the potential at node GPIO2 also low.

Fig. 2 is an equivalent diagram of plug detection circuit according to the invention with plug 20 of a typical earphone connected. Plug 20 of a typical earphone is a three-wire plug having a first conductive ring 11, as shown in Fig.2. When plug 20 of the typical earphone is connected to the earphone jack, the first conductive ring 11 of plug 20 is coupled to ground, pin 2 is coupled to pin 4 through the first conductive ring 11 of plug 20 and ground ring 10. Thus, pin 2 is grounded, and potential at node P1 grounded. Further, switch S1 is turned off, and the potential at node GPIO2 is high. In addition, pin 1 is separated from pin 3, and pin 5 is separated from pin 6 by insertion of plug 20. The voltage source Vcc charges capacitor C2 through the resistor R1 and R2. Finally, the capacitor C2 is charged to the voltage source Vcc, and the potential at node GPIO1 is high. Therefore, the potentials at nodes GPIO1 and GPIO2 of the detection circuit are both high only when plug 20 of a typical earphone is connected to the earphone jack.

Fig. 3 is an equivalent diagram of plug detection circuit according to the invention with earphone plug 30 having microphone function connected. Plug 30 with microphone function and plug 20 of the typical earphone shown in Fig. 2 is that plug 30 not only has a first conductive ring 11 but also a second conductive ring 12. When plug 30 is connected to the earphone jack, the resistor R4 is coupled to the second conductive ring 12, the potential at node P1 is a divided-voltage produced by the resistors R4 and input impedance of the second

conductive ring 12. A low pass filter consists of the resistor R5 and the capacitor C2, and the potential at node P1 is regarded as high if the input impedance of the second conductive ring 12 exceeds the resistance of the resistor R4. In addition, pin 1 is separated from pin 3, and pin 5 is separated from pin 6 due to the insertion by plug 30. At this time, the voltage source charges the capacitor C1 through the resistor R1 and R2. Finally, the potential across the capacitor is increased to the voltage source Vcc, and the potential at node GPIO1 is high.

Fig. 4 shows the relationship between the detection result, the first logic potential, and the second logic potential. As shown in Fig. 4, the potentials at nodes GPIO1 and GPIO2 are both low when no plug is connected to the earphone jack. The potentials at nodes GPIO1 and GPIO2 are both high when a plug of a typical earphone is connected to the earphone jack. In addition, the potentials at nodes GPIO1 and GPIO2 are high and low respectively when a plug of an earphone with microphone function is connected to the earphone jack.

Therefore, the present invention can detect whether a plug connected is of a typical earphone or a compound earphone with microphone function, according to the potentials at the nodes GPIO1 and GPIO2, and enable use of both types.

Although the present invention has been described in its preferred embodiments, it is not intended to limit the invention to the precise embodiments disclosed herein. Those who are skilled in this technology can

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still make various alterations and modifications without departing from the scope and spirit of this invention. Therefore, the scope of the present invention shall be defined and protected by the following claims and their equivalents.